

B1  
cont.

printing is provided to said part of said main surface of said first semiconductor

wafer.

subcl  
B2

8. (Amended) A semiconductor wafer comprising:  
no buried in. layer  
first and second semiconductor wafers having bulk structures, said first and second semiconductor wafers including main surfaces to which a semiconductor that is a material of said bulk structures is exposed,  
wherein said main surfaces of said first and second semiconductor wafers are bonded with crystal orientations shifted from each other.

#### REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-10 are presently active in this case. Claims 5 and 8 have been amended by way of the present amendment.

In the outstanding Office Action, Claim 5 was objected to for having an informality; Claims 8-10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Figures 20 and 21 of "the acknowledged prior art (APA)." Claims 1-7 were indicated as being in condition for allowance. Applicants acknowledge with appreciation the indication of allowable subject matter.

In response to the objection to Claim 5, Claim 5 has been amended as recommended in the Office Action. No further objection on this basis is therefore anticipated.

Applicants respectfully traverse the Examiner's rejection of Claims 8-10. Claims 8-10 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Figures 20-21 of the APA. However, Applicants respectfully submit that Figure 20 merely shows one wafer 30 and fails

to show the requirement of “first and second semiconductor wafers” (two wafers) recited in Claim 8 of the present invention.

Further, because of a description at page 4, lines 18-24 of the present specification that “ it is proposed that only a wafer for an SOI layer to be a wafer for the device formation is rotated by 45 degrees and is bonded to a wafer for the support substrate, thereby manufacturing an SOI wafer. As shown in Fig. 21, it is preferable that an SOI wafer 500 should be manufactured by bonding the wafer 30 for an SOI layer --- to the wafer 1 for the support substrate....” (emphasis added), the wafer shown in Figure 21 clearly has an SOI structure (Silicon on Insulator: wafer structure in which a supporting substrate, a buried insulating layer, and a silicon layer are stacked in this order).

On the other hand, “first and second semiconductor wafers having bulk structures, said first and second semiconductor wafers including main surfaces to which a semiconductor that is a material of said bulk structures is exposed” recited in the amended Claim 8 refers to two wafers not comprised of stacked films different in material. This is evident from a description at page 19, lines 8-14 of the present specification that “--- The semiconductor wafer 300 is a bulk wafer, --- In the semiconductor wafer 300, for example, a device formation layer 32 is formed on one main surface of a wafer 11 for the support substrate formed of a silicon substrate. The device formation layer 32 is provided by bonding a wafer for the device formation formed of the silicon substrate to the wafer 11 for the support substrate and then removing a part thereof, for example.” Furthermore, it is evident from a sectional view shown in Figure 6 where a buried insulating layer such as an oxide film layer 2 in Figure 2 is not formed.

Therefore, Applicants respectfully submit that the semiconductor wafer of Claim 8 having no buried insulating layer is structurally different from the SOI wafer shown in Figure 21 having a buried insulating layer. Hence, the outstanding rejection is traversed.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application and the present application is believed to be in condition for formal allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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IN THE CLAIMS

--5. (Amended) A semiconductor wafer comprising:

a first semiconductor wafer; and

a second semiconductor wafer having a crystal orientation display section to be a nick indicative of a crystal orientation formed on a fringe,

wherein said first and second semiconductor wafers are bonded to each other such that a part of a main surface of said first semiconductor wafer is exposed [to] by said crystal orientation display section of said second semiconductor wafer, and

printing is provided to said part of said main surface of said first semiconductor wafer.

8. (Amended) A semiconductor wafer comprising:

first and second semiconductor wafers having bulk structures, said first and second semiconductor wafers including main surfaces to which a semiconductor that is a material of said bulk structures is exposed,

wherein said main surfaces of said first and second semiconductor wafers are bonded with crystal orientations shifted from each other.--